
Type Designation in Accordance with Pro Electron

1 Type Designation in Accordance with Pro Electron

This type designation applies to small-signal semiconductor components – in contrast to integrated circuits, multiples of these components and semiconductor chips.

The number of the basic type consists of: two letters and a three-digit code.

First Letter

gives information about the material.

- A. Germanium or other material with a band gap of 0.6 ... 1.0 eV
- B. Silicon or other material with a band gap of 1.0 ... 1.3 eV
- C. Gallium-arsenide or other material with a band gap of 1.3 eV
- R. Compound material, e.g. cadmium-sulfide

Second Letter

Indicates the function for which the device is primarily designed.

- A. Diode: signal, low power
- B. Diode: variable capacitance
- C. Transistor: low power, audio frequency
- D. Transistor: power, audio frequency
- E. Diode: tunnel diode
- F. Transistor: low power, high frequency
- G. Multiple of dissimilar devices; miscellaneous devices (e.g. oscillator)
- H. Diode: magnetic sensitive
- L. Transistor: power, high frequency
- N. Optocoupler
- P. Radiation-sensitive semiconductor component
- Q. Radiation-emitting semiconductor component
- R. Control or switching device: low power (e.g. thyristor)
- S. Transistor: low power, switching
- T. Control or switching device: power (e.g. thyristor)
- U. Transistor: power switching
- X. Diode: multiplier, e.g. varactor, step recovery
- Y. Diode: rectifier, booster
- Z. Diode: voltage reference or regulator; transient voltage suppressor diode

The three-digit code of the type designation consists of:

- a three-digit number, running from 100 to 999, for devices primarily intended for consumer equipment etc.
- one letter and a two-digit number for devices primarily intended for industrial/professional equipment. This letter has no fixed meaning.

Notation of the Symbols and Terms Used (DIN 41 785)

2 Notation of the Symbols and Terms Used (DIN 41 785)

The current, voltage, power (AC, DC, or average values) and resistance types (AC or DC values) are indicated by using capital and small letters for the symbols.

Symbols

The instantaneous data of values varying with time are indicated by small letters.

Examples: i , v , p

Capital letters are used for DC, average, rms, and peak values of periodical functions of the current, the voltage, and the power – i.e. for constant quantities.

Examples: I , V , P

Subscripts for the Symbols

The following subscripts are used:

E, e	Emitter
B, b	Base
C, c	Collector
F, f	Forward direction (diode operated in forward direction)
R, r	Reverse direction (diode operated in reverse direction)
M, m	Peak value
av	Average value

The subscripts for peak and average values may be omitted provided that a confusion with other values is impossible.

Total values (instantaneous values, DC values, average, rms, and peak values) referred to a zero point are indicated by subscripts with capital letters.

Examples: i_C , I_C , v_{BE} , V_{BE} , p_C , P_C

Subscripts with small letters are used for the values of variable components (e.g. for instantaneous values, peak, and rms values referred to an average value).

Examples: i_c , I_c , v_{be} , V_{be} , p_c , P_c

To distinguish between peak, average, and rms values, further subscripts may be added. The following abbreviations are recommended:

Peak values	M, m
Average values	Av, av

Examples: I_{CM} , I_{CAV} , I_{cm} , I_{cav}

Peak values may also be indicated by placing the symbol “ Δ ” over the letter.

Examples: \hat{I}_C , \hat{I}_c

3 Maximum Ratings

The maximum ratings specified are absolute ratings which, if exceeded, may result in the destruction or permanent functional impairment of the component. When testing the component, as for example in respect to breakdown voltages, or during application, protection is to be provided in order to reliably ensure that maximum ratings are not exceeded.

4 Characteristics

Typical characteristics describe the component behavior at defined operating conditions. The numerical values and diagrams pertain to the component type and shall not be considered as characteristics of an individual component. The minimum and maximum ratings stated for reasons of essential quality and application requirements describe the actual spread of the characteristics, whereas spread curves in diagrams usually specify the spread range which is to be expected. Electrical values are grouped into “static” DC values and “dynamic” AC values. The thermal resistance is closely related to the maximum ratings and, constituting the upper spread value, comes immediately after the maximum ratings. The component's case data is defined by reference to standard sheets and dimensional drawings.

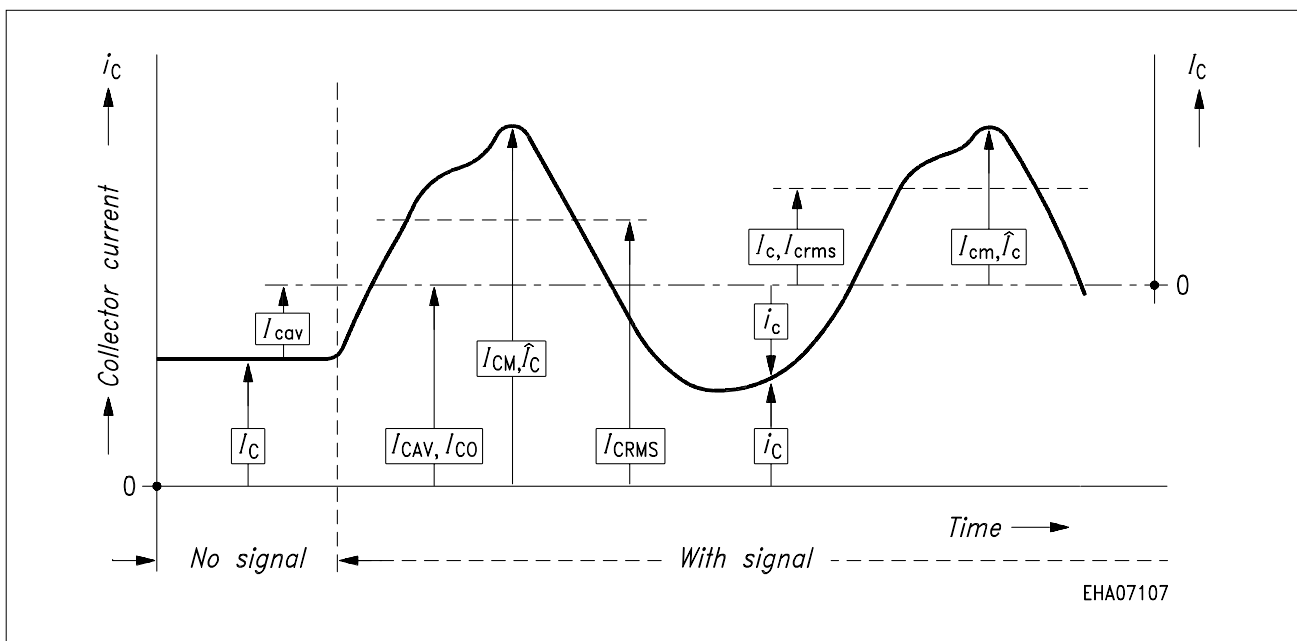


Figure 1

- I_C DC value, no signal
- I_{CAV} Average value of the total current (referred to zero)
- I_{CM}, \hat{I}_C Peak value of the total current (referred to zero)
- I_{CRMS} RMS value of the total current (referred to zero)

Characteristics

- I_{cav} Average value of the variable component superimposed on the closed-circuit direct current I_{C} (referred to the DC no-signal value I_{C})
- $I_{\text{C}}, I_{\text{crms}}$ RMS value of the variable component (referred to the average value I_{CAV})
- $I_{\text{cm}}, \hat{I}_{\text{C}}$ Peak value of the variable component (referred to the average value I_{CAV})
- i_{C} Instantaneous total value (referred to zero)
- i_{c} Instantaneous value of the variable component (referred to the average value I_{CAV})

The following relations apply to the values indicated in the above-mentioned diagram:

$$I_{\text{CAV}} = I_{\text{C}} + I_{\text{cav}}$$

$$\hat{I}_{\text{CM}} = I_{\text{C}} = I_{\text{CAV}} + I_{\text{cm}}$$

$$I_{\text{CRMS}} = \sqrt{I_{\text{CAV}}^2 + I_{\text{crms}}^2}$$

$$I_{\text{C}} = I_{\text{CAV}} + i_{\text{C}}$$

Basic Symbol Chart

The following chart illustrates the application of capital and small letter symbols.

Table 1

		Symbols	
		i, v, p	I, V, P
Subscripts	e b c f r m av	Instantaneous value of the variable component	RMS, average, and peak value of the variable component
	E B C F R M AV	Instantaneous total value (as referred to zero)	DC value, average, rms, and peak value (as referred to zero)

Instructions for the Subscript Sequence

Voltages

As a rule, two subscripts are used to indicate the points between which the voltage is measured.

Positive numerical values of the voltages correspond to positive potentials on the point indicated by the first subscript as referred to the point indicated by the second subscript (point of reference).

The second subscript may be omitted if this cannot lead to confusion or misunderstandings.

A supply voltage may be indicated by repeating the subscript of the terminal concerned.

Examples: V_{EEB} , V_{BBC} , V_{CCE}

Currents

As a rule, at least one subscript is used. Positive numerical values of the current correspond to positive currents entering the component at the terminal indicated by the first subscript.

Subscripts for Terminals

In the case of components having more than one terminal of the same type, the subscripts for the terminals may be modified by suffixing a number to them. Subscript and suffix must be written on the same line.

Example: V_{B2-E} (voltage between second base terminal and emitter)

If several components form an assembly, the subscripts for the terminals may be modified by prefixing a number to them, subscript and prefix having to be written on the same line.

Example: V_{1B-2B} (voltage between the base of the first component and the base of the second component)

Admittances, Resistances, Four-Pole Network Coefficients, etc.

Symbols

Small letters with appropriate subscripts are used for four-pole network coefficients, as well as resistances, admittances, capacitances, inductances, etc., which describe the features of the component.

Examples: h_{11b} , h_{11e} , z_{21b} , y_{22c}

Characteristics

Capital letters with appropriate subscripts are used for four-pole network coefficients, as well as resistances, admittances, capacitances, inductances, etc. of external network or of networks in which the component forms just a part.

Examples: H_{11b} , H_{11e} , Z_{21b} , Y_{22c}

Capital-letter subscripts are used for DC values (including large-signal values) of four-pole network coefficients, as well as, of resistances, admittances, etc.

The DC value is the slope of the straight line from the origin of the coordinate system to the operating point on the characteristic of the component.

Examples: r_B , h_{11B} , h_{FE}

Small-letter subscripts are used for AC values (small-signal values) of four-pole network coefficients, as well as of resistances, admittances, capacitances, inductances, etc.

Examples: r_{bb} , h_{11b} , h_{fe}

The first subscript or the first pair of subscripts written in the manner customary for matrix elements is used for determining the elements of a four-pole network matrix.

11 (or i) = input
 22 (or o) = output
 21 (or f) = forward transfer

12 (or r) = reverse transfer

Examples: $V_1 = h_{11} \times I_1 + h_{12} \times V_2$
 $I_2 = h_{21} \times I_1 + h_{22} \times V_2$

Note

When written in matrix representation (or as elements of matrixes) the voltage and current symbols are supplemented by a subscript consisting of a single numeral.

Subscript 1 = input
 Subscript 2 = output

The second subscript or the subscript following the pair of numerals indicates the basic circuit. If the common terminal is self-evident, the second subscript may be omitted

e = common emitter configuration
 b = common base configuration
 c = common collector configuration

Examples: (common base configuration)

$$I_1 = y_{11b} \times V_{1b} + y_{12b} \times V_{1b}$$

$$I_2 = y_{21b} \times V_{1b} + y_{22b} \times V_{2b}$$

If the transistor is described with a four-pole characteristic, it is recommended to fix the direction arrows for the input and output currents in the direction of the four-pole network.

Alphanumerical List of the Symbols Used

5 Alphanumerical List of the Symbols Used

a	On-off base current ratio
A	Anode
A	Static current gain in common base configuration
α	Dynamic short-circuit current gain in common base configuration
b	Imaginary part of y-parameters
b_{11}	Imaginary part of the short-circuit input admittance (of parameter y_{11})
b_{12}	Imaginary part of the short-circuit reverse transfer admittance (of parameter y_{12})
b_{21}	Imaginary part of the short-circuit forward transfer admittance (of parameter y_{21})
b_{22}	Imaginary part of the short-circuit output admittance (of parameter y_{22})
B, b	Base terminal
C, c	Collector terminal
C	Capacitance
$C_{b'c}$	Intrinsic base collector capacitance
$C_{b'e}$	Intrinsic base emitter capacitance
C_c	Collector junction capacitance (in general)
C_{case}	Case capacitance (in general)
C_{cb}	Collector base capacitance
C_{CBO}	Collector base capacitance (including case capacitance) with open emitter ($I_E = 0$)
$C_{c'b}$	Intrinsic collector base capacitance
C_{ce}	Collector-emitter capacitance
C_{dg1}	Reverse transfer capacitance
C_{dss}	Output capacitance
C_{eb}	Emitter-base capacitance
C_{EBO}	Emitter-base capacitance (including case capacitance) with collector open ($I_C = 0$)
$C_{e'b}$	Intrinsic emitter base capacitance
C_{g1ss}	Gate1 input capacitance
C_{g2ss}	Gate2 input capacitance
C_{ib}	Input capacitance
C_L	Load capacitance
C_{ob}	Output capacitance
C_{th}	Thermal capacity (disregarding of heat dissipation to the environment)
C_T	Diode capacitance
C_{T1}/C_{T28}	Capacitance ratio ($C_T (V_R = 1 \text{ V}) / C_T (V_R = 28 \text{ V})$)
$\Delta C_T/C_T$	Capacitance matching
C_{11}	Capacitance of the short-circuit input admittance (of parameter y_{11})

Alphanumerical List of the Symbols Used

C_{12}	Capacitance of the short-circuit reverse transfer admittance (of parameter y_{12})
C_{21}	Capacitance of the short-circuit forward transfer admittance (of parameter y_{21})
C_{22}	Capacitance of the short-circuit output admittance (of parameter y_{22})
D	Duty cycle $D = t_p / T$
E, e	Emitter terminal
Δf	Frequency difference
f	Frequency
f_c	Cutoff frequency
f_{hfb}	Cutoff frequency of the short-circuit small signal current gain in common base configuration
f_{hfe}	Cutoff frequency of the short-circuit small signal current gain in common emitter configuration
f_{hfe1}	Frequency at which $h_{fe} = 1$
f_{max}	Maximum frequency of oscillation
f_T	Transition frequency (Current gain-bandwidth product)
F	Noise figure
g	Real part of the y-parameters
g	Conductance (instantaneous value)
$g_{b'c}$	Intrinsic base collector conductance
$g_{b'e}$	Intrinsic base emitter conductance
g_{ce}	Collector emitter conductance
$g_m; g_{fs}$	Transconductance
g_{th}	Coefficient of thermal conductivity (instantaneous total value)
g_{thJC}	Coefficient of thermal conductivity (total instantaneous value) between heat source and case, with infinitely good heat dissipation from the case ($T_{case} = T_{amb}$)
g_{11}	Real component of the short-circuit input admittance (of parameter y_{11})
g_{12}	Real component of the short-circuit reverse transconductance (of parameter y_{12})
g_{21}	Real component of the short-circuit forward transconductance (of parameter y_{21})
g_{22}	Real component of the short-circuit output admittance (of parameter y_{22})
G	Conductance (DC or average value)
ΔG	Gain flatness
G_a	Associated gain
G_g	Internal conductance of generator
G_L	Load conductance

Alphanumerical List of the Symbols Used

G_{ma}	Power gain (Maximum available gain)
G_{ms}	Power gain (Maximum stable gain)
ΔG_p	Gain control range
G_p	Power gain
G_{pb}	Power gain in common base configuration
G_{pe}	Power gain in common emitter configuration
G_{popt}	Power gain, optimum
G_{pbinv}	Reverse power loss (feedback damping)
G_{pbopt}	Power gain in common base configuration, optimum
G_{peopt}	Power gain in common emitter configuration, optimum
G_{th}	Coefficient of thermal conductivity (thermal conduction constant)
G_{thA}	Coefficient of thermal conductivity (thermal conduction constant) between heat source and static ambient air when using a cooling plate of defined size
G_{thJA}	Coefficient of thermal conductivity (thermal conduction constant) between heat source and static ambient air.
G_{thJC}	Coefficient of thermal conductivity (thermal conduction constant) between heat source and case, with infinitely good heat dissipation from the case ($T_{case} = T_{amb}$)
G_V	Voltage gain
Γ_{opt}	Reflection coefficient for minimum noise
h	Parameter of the hybrid-matrix (h -matrix)
h_{11}	Short-circuit input impedance
h_{12}	Open-circuit reverse voltage transfer ratio (voltage feedback ratio h_{re})
h_{21}	Short-circuit forward current transfer ratio (small signal current gain)
h_{22}	Open-circuit output admittance
h_{FE}	DC current gain in common emitter configuration (static forward current transfer ratio)
h_{fe}	Small-signal current gain in common emitter configuration ($\beta = h_{21e}$)
h_{feo}	Small-signal current gain in common emitter configuration at $f = 1$ kHz (Dynamic short-circuit forward current transfer ratio in common emitter configuration)
i_1	Input AC current
i_2	Output AC current (in general)
I_B	Base current (DC or average value)
I_{B1}	Control current, base-one current (UJT)
I_{B2}	Turn-off base current, on-off base current (UJT)
I_{BM}	Peak base current
I_C	Collector current (DC or average value)
I_{CBO}	Collector cutoff current with open emitter ($I_E = 0$)
I_{CEO}	Collector cutoff current with open base ($I_B = 0$)

Alphanumerical List of the Symbols Used

I_{CER}	Collector cutoff current with $R_{\text{BE}} = R$ (with a resistance R_{BE} between base and emitter)
I_{CES}	Collector cutoff current with short-circuited emitter diode ($V_{\text{BE}} = 0$)
I_{CEV}	Collector cutoff current with reverse emitter diode
I_{CM}	Peak collector current
I_{D}	Drain current
I_{DSS}	Drain source saturation current
I_{E}	Emitter current (DC or average value)
I_{EBO}	Emitter cutoff current with open collector ($I_{\text{C}} = 0$)
I_{EM}	Peak emitter current
I_{F}	Forward current
I_{FM}	Peak forward current
I_{FS}	Surge current, maximum 1 sec
I_{G}	Gate leakage current
$\pm I_{\text{G1SS}}$	Gate1-source leakage current
$\pm I_{\text{G2SS}}$	Gate2-source leakage current
I_{K}	Short-circuit current
I_{o}	Rectified current
I_{R}	Reverse current
IP_3	Third order intercept point
k	Stability factor
K	Cathode
L	Inductance
L_{s}	Series inductance
m	In a subscript: maximum (peak value)
m	Degree of modulation
max	In a subscript: maximum (e.g. upper scattering limit)
min	in a subscript: minimum (e.g. lower scattering limit)
M	in a subscript: maximum (peak value)
NF, F	Noise figure
$NF_{\text{min}}, F_{\text{min}}$	Minimum noise figure
$NF_{50\Omega}, F_{50\Omega}$	Noise figure 50 Ω –System
$P; p$	Power dissipation
PAE	Power added efficiency
P_{p}	Pulse power dissipation
P_{tot}	Total power dissipation
$P_{-1\text{dB}}$	RF output power at 1 dB compression point

Alphanumerical List of the Symbols Used

φ	Phase of y-parameters
φ_{11}	Phase of the short-circuit input admittance (of parameter y_{11})
φ_{12}	Phase of the short-circuit reverse transfer admittance (of parameter y_{12})
φ_{21}	Phase of the short-circuit forward transfer admittance (of parameter y_{21})
φ_{22}	Phase of the short-circuit output admittance (of parameter y_{22})
Q	Q factor (Quality factor)
r	Resistance (instantaneous value)
$r_{bb'}$	Base intrinsic resistance
$r_{bb'} C_{b'c}$	Feedback time constant
r_{cc}	Collector intrinsic resistance
r_{eb}	Emitter intrinsic resistance
r_f	Forward resistance of diodes
R	Resistance (DC or average value)
R_{BE}	Resistance between base and emitter
R_g	Internal resistance of generator
R_L	Load resistance
R_N	Equivalent noise resistance
r_N	Normalized equivalent noise resistance
R_s	Series resistance
R_{th}	Thermal resistance
R_{thc}	Thermal resistance of a chassis plate (cooling plate, no heat sink)
R_{thJA}	Thermal resistance between junction (heat source) and static ambient air
R_{thJS}	Thermal resistance between junction and soldering point
R_{thJT}	Thermal resistance between junction and Chip base (Chip thermal resistance)
R_{thTS}	Thermal resistance between chip base and soldering point (package / alloy layer)
R_{thSA}	Thermal resistance between soldering point and ambient (substrate thermal resistance)
R_{thJC}	Thermal resistance between junction (heat source) and case at infinitely good heat dissipation from the case ($T_{case} = T_{amb}$)
R_O	Differential resistance
$ S_{21} ^2$	Power gain in 50 Ω -system
S_{11}	Input reflection coefficient in 50 Ω -system
S_{21}	Forward transmission coefficient in 50 Ω -system
S_{12}	Reverse transmission coefficient in 50 Ω -system
S_{22}	Output reflection coefficient in 50 Ω -system

Alphanumerical List of the Symbols Used

t	Time
t_d	Delay time
t_f	Fall time
t_{gt}	Gate controlled turn-on time
t_{gq}	Gate controlled turn-off time
t_h	In a subscript: thermal
t_{off}	Turn-off time ($t_{off} = t_s + t_f$)
t_{on}	Turn-on time ($t_{on} = t_d + t_r$)
t_p	Pulse duration
t_q	Circuit commutated turn-off time
t_r	Rise time
t_{rr}	Reverse recovery time
t_s	Storage time
T	Temperature
T	Period duration
T_{amb}	Ambient temperature
T_{case}	Case temperature
T_{Ch}	Channel temperature
T_j	Junction temperature
Tr	Abbreviation for “transistor”
T_S	Soldering point temperature
T_{stg}	Storage temperature
τ	Charge carrier life time
v	Voltage (instantaneous value)
v_{FM}	Peak forward voltage
v_{RF}	Input RF voltage
v_{RM}	Peak reverse voltage
v_{RS}	Maximum surge voltage, 1 sec
v_1	Input AC voltage
v_2	Output AC voltage
V	Voltage
V_{batt}	Battery voltage
V_{BB}	Base supply voltage
V_{BE}	Base emitter voltage
$V_{(BR)} \dots$	Breakdown voltage
$V_{(BR) DS}$	Drain-Source-breakdown voltage
$\pm V_{(BR) G1SS}$	Gate1-Source-breakdown voltage
$\pm V_{(BR) G2SS}$	Gate2-Source-breakdown voltage
$-V_{G1S(P)}$	Gate1-Source Pinch-off voltage
$-V_{G2S(P)}$	Gate2-Source Pinch-off voltage
V_{CB}	Collector base voltage
V_{CBO}	Collector-base voltage with open emitter ($I_E = 0$)

Alphanumerical List of the Symbols Used

V_{CC}	Collector supply voltage
V_{DS}	Drain-source voltage
V_{DG}	Drain-gate voltage
V_{GS}	Gate-source voltage
V_{CE}	Collector emitter voltage
V_{CEO}	Collector-emitter (reverse) voltage base open ($I_B = 0$)
V_{CER}	Collector-emitter (reverse) voltage with a resistor between base and emitter
V_{CES}	Collector-emitter voltage with short-circuited emitter diode ($V_{BE} = 0$)
V_{CEsat}	Collector-emitter saturation voltage
V_{CEV}	Collector-emitter (reverse) voltage with reverse base emitter diode
V_{IN}	Input voltage
V_{EBO}	Emitter-base voltage with open collector ($I_C = 0$)
V_F	Forward voltage
$V_{GS(P)}, V_P$	Pinch-off voltage
V_O	Open-circuit voltage
V_{OUT}	Output voltage
V_t	Tuning voltage
Y	Parameter of the admittance matrix (y-matrix)
Y_{11}	Short-circuit input admittance
Y_{12}	Short-circuit reverse transfer admittance
Y_{21}	Short-circuit forward transfer admittance
Y_{22}	Short-circuit output admittance
z_{12}	Reverse impedance with open input
Z_1	Input impedance (general)
Z_2	Output impedance (general)
η	Collector or drain efficiency
ω	Angular frequency $\omega = 2 \times \pi \times f$

Explanation of the Symbols and Terms Used

6 Explanation of the Symbols and Terms Used

This section contains brief explanations of the symbols and terms used in the data sheets for transistors.

In order to distinguish between the different voltages and currents of the transistor, suffix letters are used.

The letters provide information on the connection mode of the transistor terminals. The order on which they are indicated together with the sign (+ or –) indicates the direction of the voltage or current. The technical concept of current flow applies (current flow from + to –).

The three transistor terminals are denoted as follows:

Emitter E

Base B

Collector C

In order to characterize the cutoff currents and reverse voltages a third suffix letter is used. This letter provides information on the connection mode of the third terminal which is otherwise not mentioned.

Following abbreviations are used:

- O The third, unmentioned terminal is open.
- R Ohmic resistance between the terminal mentioned in the second place and the unmentioned terminal.
- S Short circuit between the terminal mentioned in the second place and the unmentioned terminal.
- V Reverse bias voltage between the terminal mentioned in the second place and the unmentioned terminal.

7 Technical Explanations

7.1 Basic Transistor Configurations

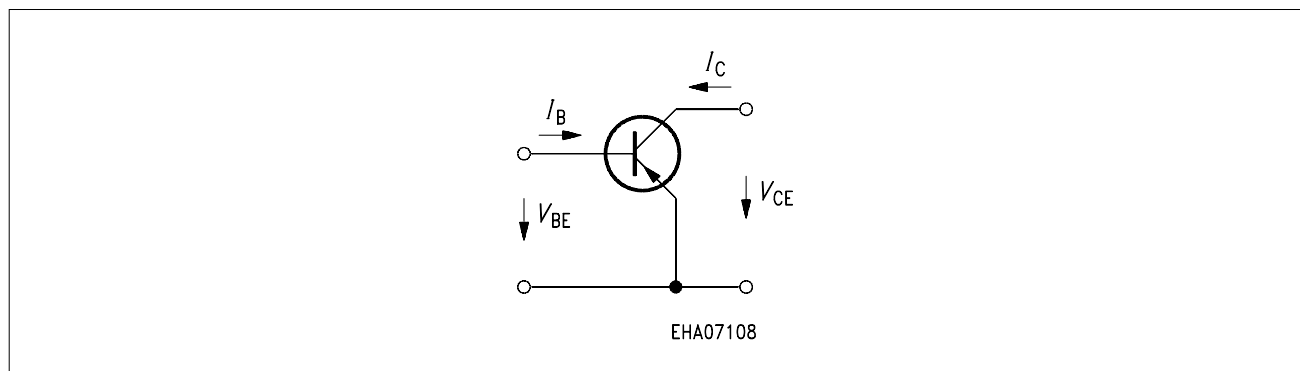


Figure 2 Common Emitter Configuration

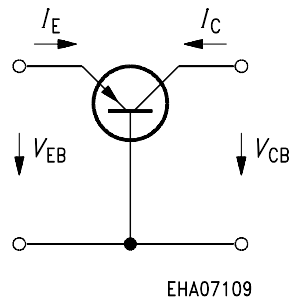


Figure 3 Common Base Configuration

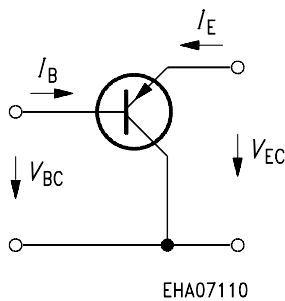


Figure 4 Common Collector Configuration

Table 2 Characteristics of the Basic Configurations

	Common Emitter Configuration	Common Base Configuration	Common Collector Configuration
Input impedance Z_1	medium Z_{1e}	low	high
Output impedance Z_2	high Z_{2e}	very high	low
Small-signal current gain	high h_{fe}	< 1	high
Voltage gain	high	high	< 1
Power gain	very high	high	medium
Cutoff frequency f_{hfe}	low	high	low

7.2 Explanations of Important Electrical Characteristics

7.2.1 DC Parameters

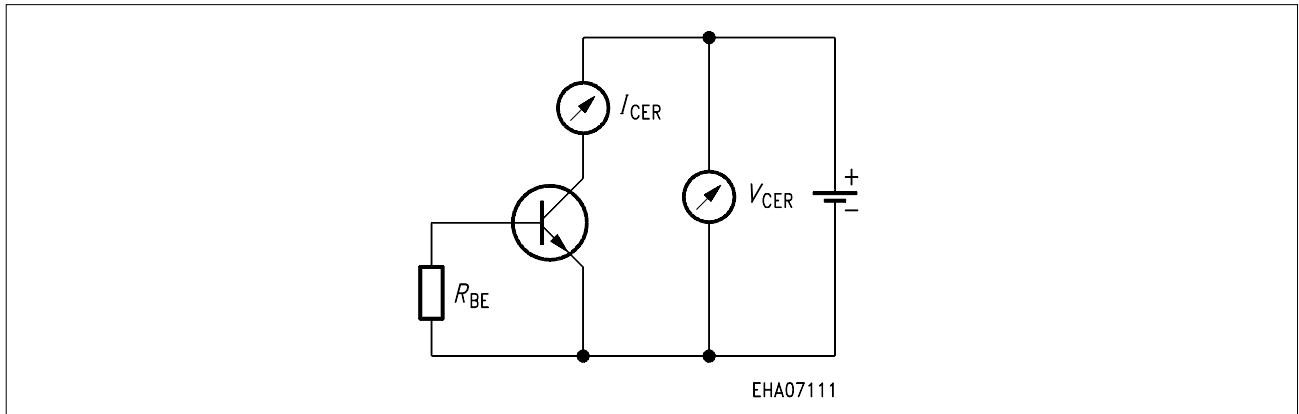


Figure 5 V_{CER} (I_{CER})

Collector-emitter reverse voltage (collector-emitter cutoff current) with a resistor between base and emitter. The maximum permissible resistance value R_{BE} is specified in the data sheets. The reverse voltage V_{CEO} applies to higher values of R_{BE} .

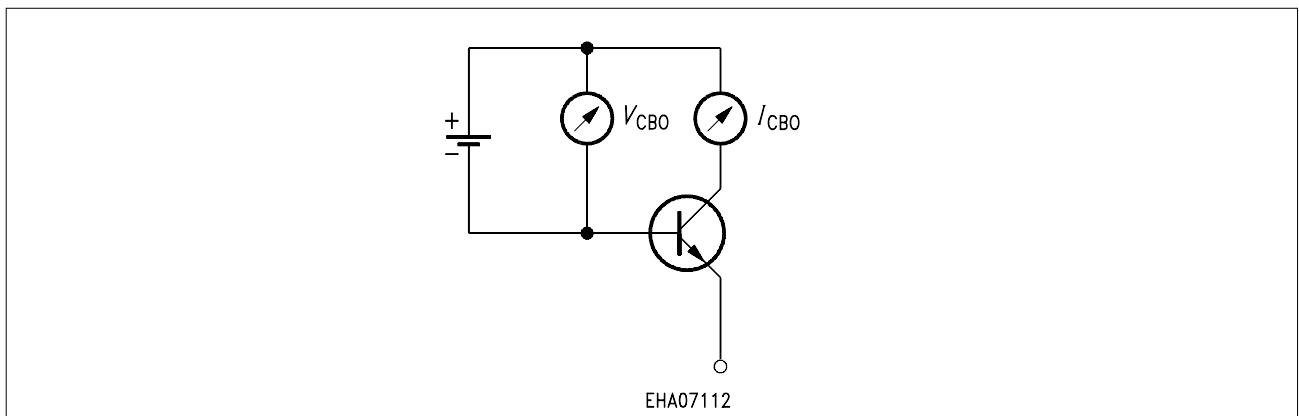


Figure 6 V_{CBO} (I_{CBO})

Collector-base reverse voltage (collector-base cutoff current) with emitter open: $I_E = 0$.

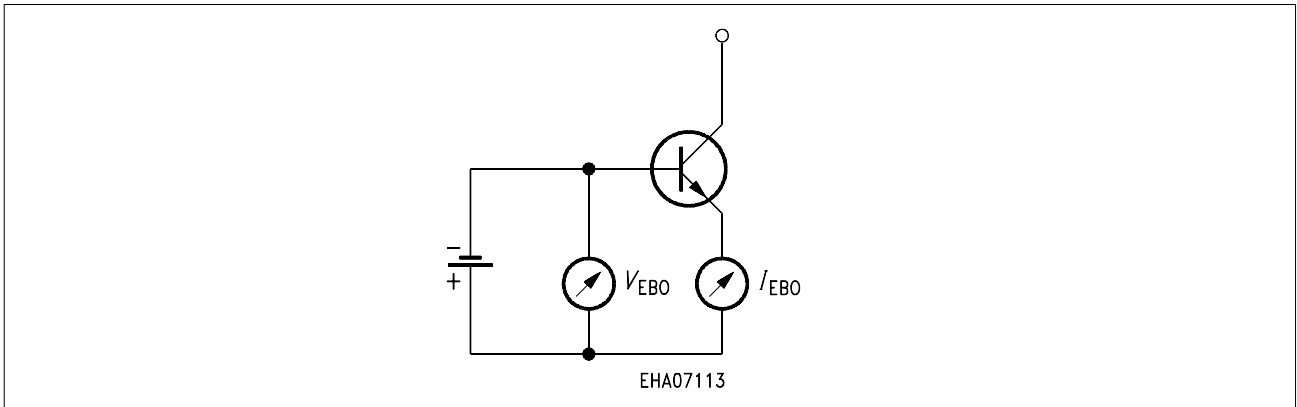


Figure 7 V_{EBO} (I_{EBO})

Emitter-base reverse voltage (emitter-base cutoff current) with collector open: $I_C = 0$.

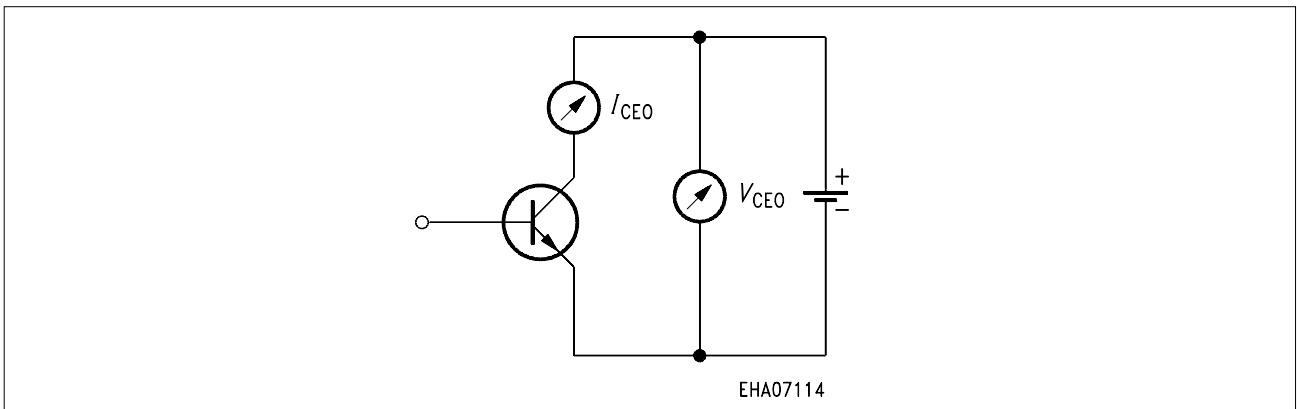


Figure 8 V_{CEO} (I_{CEO})

Collector-emitter reverse voltage (collector-emitter cutoff current) with base open: $I_B = 0$. The state $I_B = 0$ may also occur for a short while, e.g. in operation as a switch, with a resistance interposed between base and emitter.

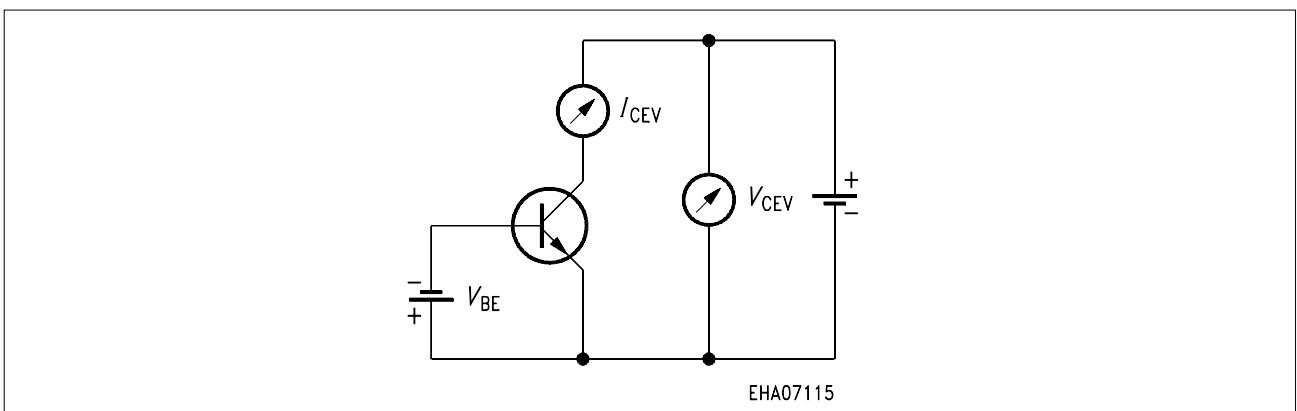


Figure 9 V_{CEV} (I_{CEV})

Collector-emitter reverse voltage (collector emitter cutoff current) with blocked emitter diode, i.e., reverse bias voltage between base and emitter.

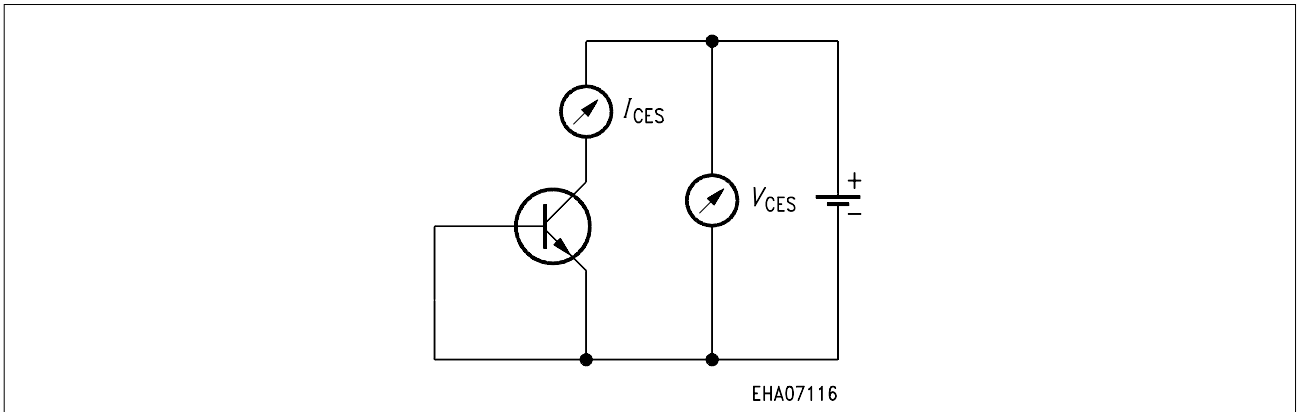


Figure 10 $V_{CES} (I_{CES})$

Collector-emitter reverse voltage (collector-emitter cutoff current) with shorted emitter diode: $V_{BE} = 0$.

7.2.2 RF Parameters

$$G_{ms} = \left| \frac{S_{21}}{S_{12}} \right| \quad G_{ma} = \left| \frac{S_{21}}{S_{12}} \right| \times (k - \sqrt{k^2 - 1})$$

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|}$$

G_{ma} , G_{ms}

Maximum available gain if $k \geq 1$

Maximum stable gain if $k < 1$

k Stability factor

$$(|S_{21}|^2)_{dB} = 10 \times \log |S_{21}|^2$$

$|S_{21}|^2$

Insertion power gain in a 50 Ω system without matching at input and output.

$$f_T = |h_{21}| \times f$$

f_T

Transition frequency, determined by S-parameter measurement and calculation.

h_{21} Current gain

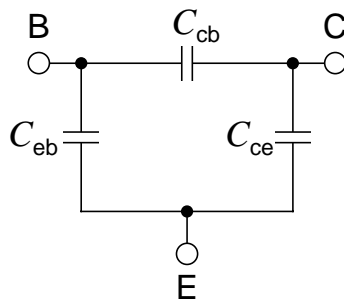
f Measurement frequency

$$PAE = \frac{P_{RF, OUT}}{P_{RF, IN} + P_{DC}} \quad \eta = \frac{P_{RF, OUT}}{P_{DC}}$$

PAE

Power Added Efficiency

η Efficiency (collector- or drain-efficiency)



C_{cb} Collector-base capacitance
 C_{ce} Collector-emitter capacitance
 C_{eb} Emitter-base capacitance

8 Thermal Resistance

The heat caused by the power loss P_{tot} in the active semiconductor region during operation results in an increased temperature of the component. The heat is dissipated from its source (junction J or channel Ch) via the chip, the case and the substrate (pc board) to the heat sink (ambient A). The junction temperature T_J at an ambient temperature T_A is determined by the thermal resistance R_{thJA} and the power dissipation P_{tot} :

$$T_J = T_A + P_{tot} \times R_{thJA}$$

(with R_{thJA} in K/W or °C/W)

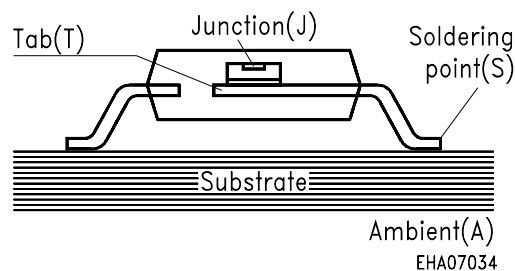


Figure 11

RF and AF Transistors and Diodes in SMD Packages

9 RF and AF Transistors and Diodes in SMD Packages

In SMD packages the heat is primarily dissipated via the pins. The total thermal resistance in this case is made up of the following components:

$$R_{thJA} = R_{thJT} + R_{thTS} + R_{thSA}$$

$$R_{thJS} = R_{thJT} + R_{thTS}$$

R_{thJA} thermal resistance between junction and ambient (total thermal resistance)

R_{thJS} thermal resistance between junction and soldering point

R_{thJT} thermal resistance between junction and chip base (chip thermal resistance)

R_{thTS} thermal resistance between chip base and soldering point (package/alloy layer)

R_{thSA} thermal resistance between soldering point and ambient (substrate thermal resistance)

R_{thJS} contains all type-dependent quantities. For a given power dissipation P_{tot} it is possible to use it to precisely determine the component temperature if the temperature T_S of the warmest soldering point is measured (for bipolar transistors typically the collector, for FETs the source lead).

$$T_J = T_S + P_{tot} \times R_{thJS}$$

The temperature of the soldering point T_S is determined by the application, i.e. by the substrate, heat produced by external components and the ambient temperature T_A . These components combine to form the substrate thermal resistance R_{thSA} that is circuit-dependent and can be influenced by heat dissipation measures.

$$T_S = T_A + P_{tot} \times R_{thSA}$$

If measurement of the temperature of the soldering point T_S is not possible, or if estimation of the junction temperature is sufficient, R_{thSA} can be read from diagrams below. Here we give an approximate value of the thermal resistance R_{thSA} between the soldering point on an epoxy or ceramic substrate and still air as a function of the area of the collector mounting or ceramic. The parameter is the dissipated power, i.e. the heat $T_S - T_A$ of the pc board. So in this case for the operating temperature:

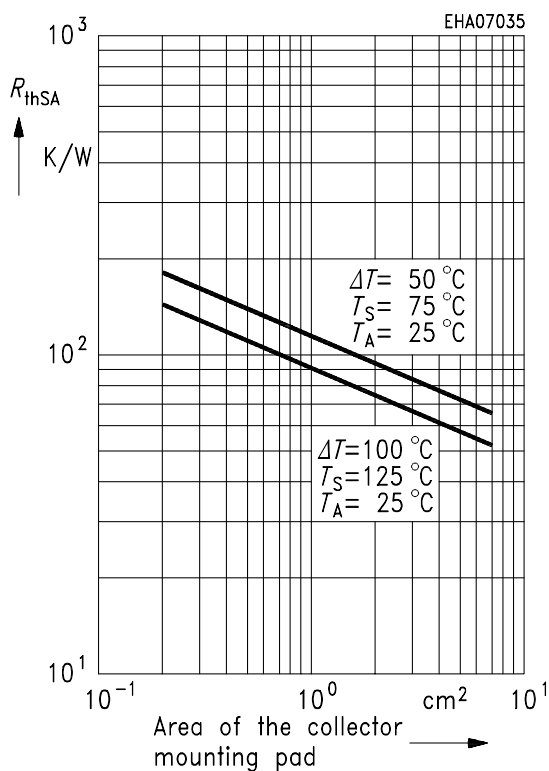
$$T_J = T_A + P_{tot} \times (R_{thJS} + R_{thSA})$$

RF and AF Transistors and Diodes in SMD Packages

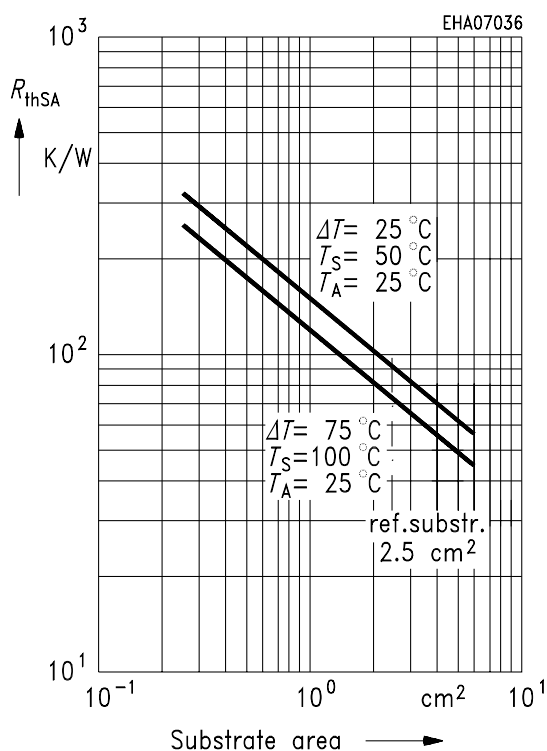
In the data sheets R_{thJS} is stated as a thermal reference quantity of the heat dissipation. The total thermal resistance R_{thJA} is stated for comparison purposes. Depending on the typical component application, substrates of the following kinds are used for reference:

- AF applications epoxy circuit board: collector mounting area in cm^2 Cu (see **data sheets**), thickness 35 μm Cu.
- RF applications ceramic substrate: 15 mm \times 16.7 mm \times 0.7 mm (alumina) or epoxy circuit board with collector mounting area corresponding to 80 K/W.

The two diagrams below show, to an approximation, the thermal resistance as a function of the substrate area, assuming that the test device is located in the center of a virtually square substrate.



Heat Dissipation from PC Board to Ambient Air (mounting pad Cu 35 μm / substrate: epoxy 1.5 mm)



Heat Dissipation from Al_2O_3 -Substrate to Ambient Air (substrate in still air, vertical 0.6 mm thick)

RF and AF Transistors and Diodes in SMD Packages

9.1 Temperature Measuring of Components Leads

Measuring with temperature indicators (e.g. thermopaper)

Temperature indicators do not cause heat dissipation and thus allow an almost exact determination of temperature. A certain degree of deviations can only result from rough-grade indication of the temperature indicators. This method is quite easy and provides sufficient accuracy. It is particularly suitable for measurement on pc boards.

Measuring with thermocouple elements

Measurement with thermocouple elements is not advisable because the functioning of the circuit can be influenced by the electrical conduction and the heat dissipation by the soldering point. This corrupts the results of the measurement, unless measurement is carried out with appropriate effort.

9.2 Permissible Total Power Dissipation in DC Operation

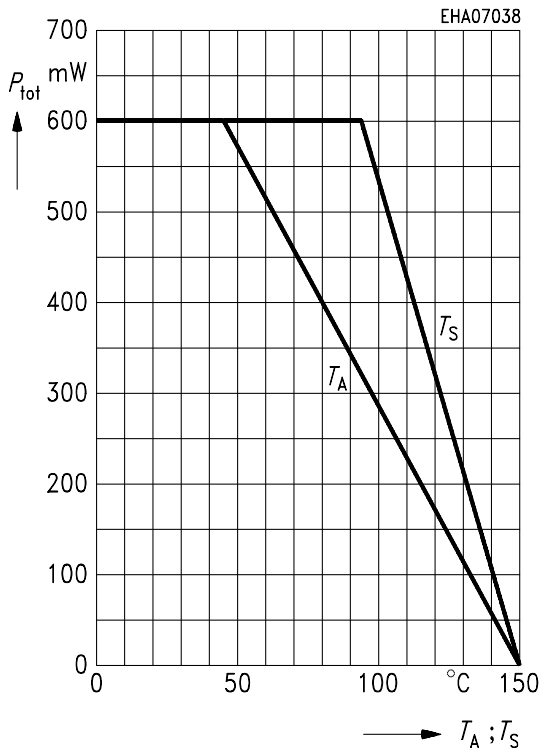
The total power dissipation P_{tot} defines the maximum thermal gradient in the component. As a result of the heating of components, the maximum total power dissipation $P_{\text{tot max}}$ stated in the data sheets is only permissible up to limits of $T_{\text{S max}}$ or $T_{\text{A max}}$. These critical temperatures describe the point at which the maximum permissible junction temperature $T_{\text{J max}}$ is reached. The maximum permissible ambient or soldering-point temperature is calculated as follows:

$$T_{\text{S max}} = T_{\text{J max}} - P_{\text{tot max}} \times R_{\text{thJS}}$$

$$T_{\text{A max}} = T_{\text{J max}} - P_{\text{tot max}} \times R_{\text{thJA}}$$

In diodes the power dissipation is for the most part caused by internal resistance. So the diagram has to be translated into the form $I_{\text{F}} = f(T_{\text{S}}; T_{\text{A}})$, resulting in the bent shape of the curve. For R_{thJA} the appropriate standard substrate was taken in each case. The diagrams shown here are intended as examples. For the application the curve given in the data sheet is to be taken. Exceeding the thermal max. ratings is not permissible because this could mean lasting degradation of the component's characteristics or even its destruction.

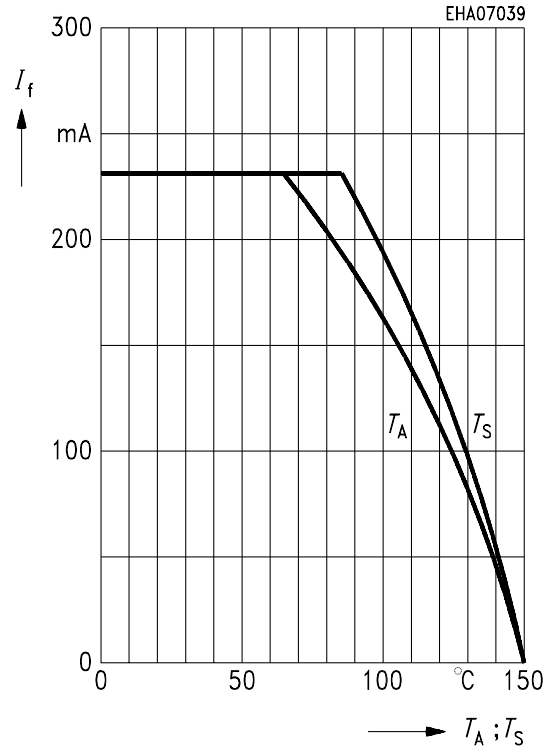
RF and AF Transistors and Diodes in SMD Packages



Total Power Dissipation

$$P_{\text{tot}} = f(T_S; T_A^{1)})$$

¹⁾ Al₂O₃-Substrate 15 mm × 16.7 mm × 0.7 mm / Package mounted on alumina 15 mm × 16.7 mm × 0.7 mm



Forward Current

$$I_F = f(T_S; T_A^{1)})$$

9.3 Permissible Total Power Dissipation in Pulse Operation

In pulse operation, under certain circumstances, higher total power dissipation than in DC operation can be permitted. This will be the case when the pulse duration t_p , i.e. the length of time that power is applied, is small compared to the thermal time constant of the system. This time constant, i.e. the time until the final temperature is reached, depends on the thermal capacitances and resistances of the components chip, case and substrate. The thermal capacitance utilized in the component is a function of the pulse duration.

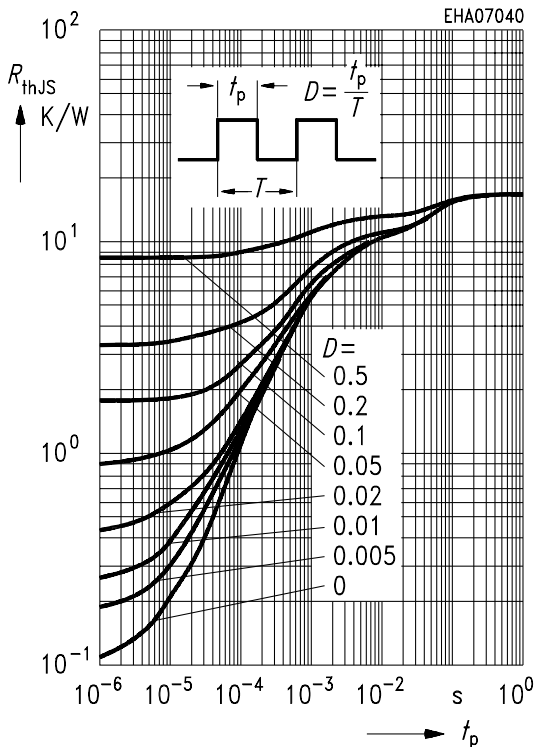
Here we describe this through the transient thermal resistance. The pulse-load thermal resistance, or the permissible increase in P_{tot} that can be derived from it, is shown by way of examples in the following curves. For the application the particular data sheet should be taken.

$$P_{\text{tot max}} / P_{\text{tot DC}} = f(t_p)$$

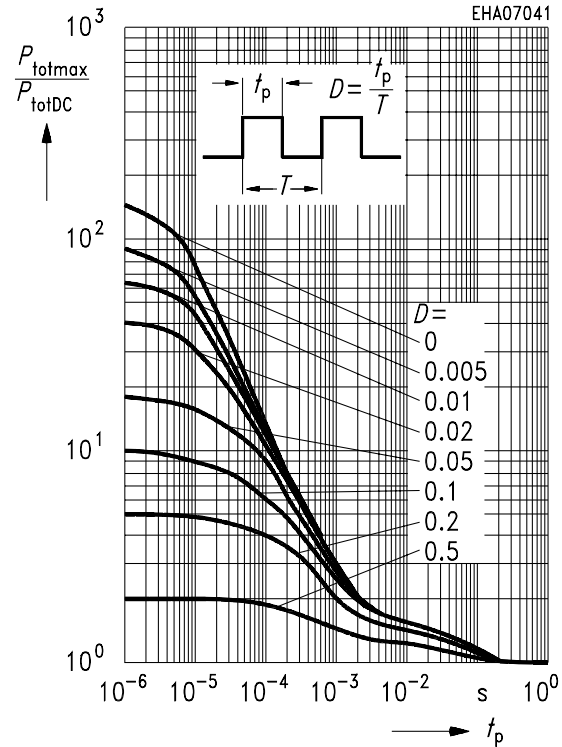
The duty factor t_p / T is given as a parameter for periodic pulse load with a period of T . For long pulse durations the factor $P_{\text{tot max}} / P_{\text{tot DC}}$ approaches a value of 1, i.e. P_{tot} in pulsed operation can be equated with the DC value. At extremely short pulse widths, on

ESD (Electrostatic Discharge Sensitive Device)

the other hand, the increase in temperature as a result of the pulse (residual ripple) becomes negligible and a mean temperature is created in the system that corresponds to DC operation with average pulse power.



Permissible Pulse Load
 $R_{thJS} = f(t_p)$



Permissible Pulse Load
 $P_{tot\ max} / P_{tot\ DC} = f(t_p)$

10 ESD (Electrostatic Discharge Sensitive Device)

ESD-sensitive components are supplied in anti-static packaging. The attached warning label calls your attention to the necessity of protecting the components against electrostatic discharge, beginning with the opening of the package.

11 Standards

For detailed information please refer to the following DIN literature:

DIN 41 782: Diodes

DIN 41 785: Maximum Ratings

DIN 41 791: General Instructions

DIN 41 852: Semiconductor Technology

DIN 41 853: Terms Relating to Diodes

DIN 41 854: Terms Relating to Bipolar Transistors